ABSTRACT

A field effect transistor formed on a SOI substrate is equipped with a gate (102) formed on a substrate, a source (103) and a drain (104) each spaced a specified distance from a crystal region below the gate, a first extension region (110) that extends in a channel formed between the source and an area below the gate, and a second extension region (111) that extends in a channel formed between the drain and an area below the gate, wherein junction depths (Xs, Xd) of the first and second extension regions is formed shallower than junction depths (Xt) of the source region (103) and the drain region (104).